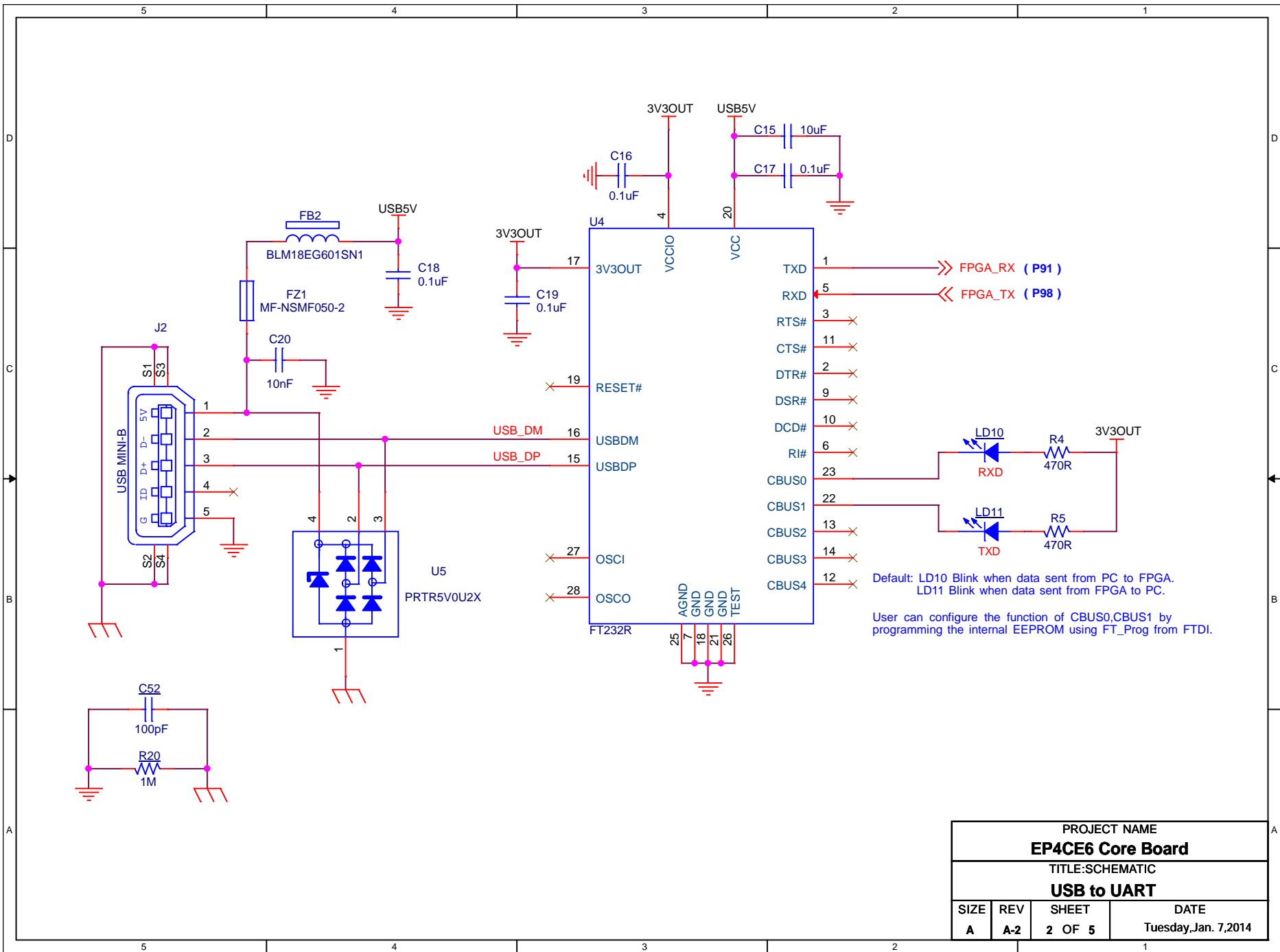
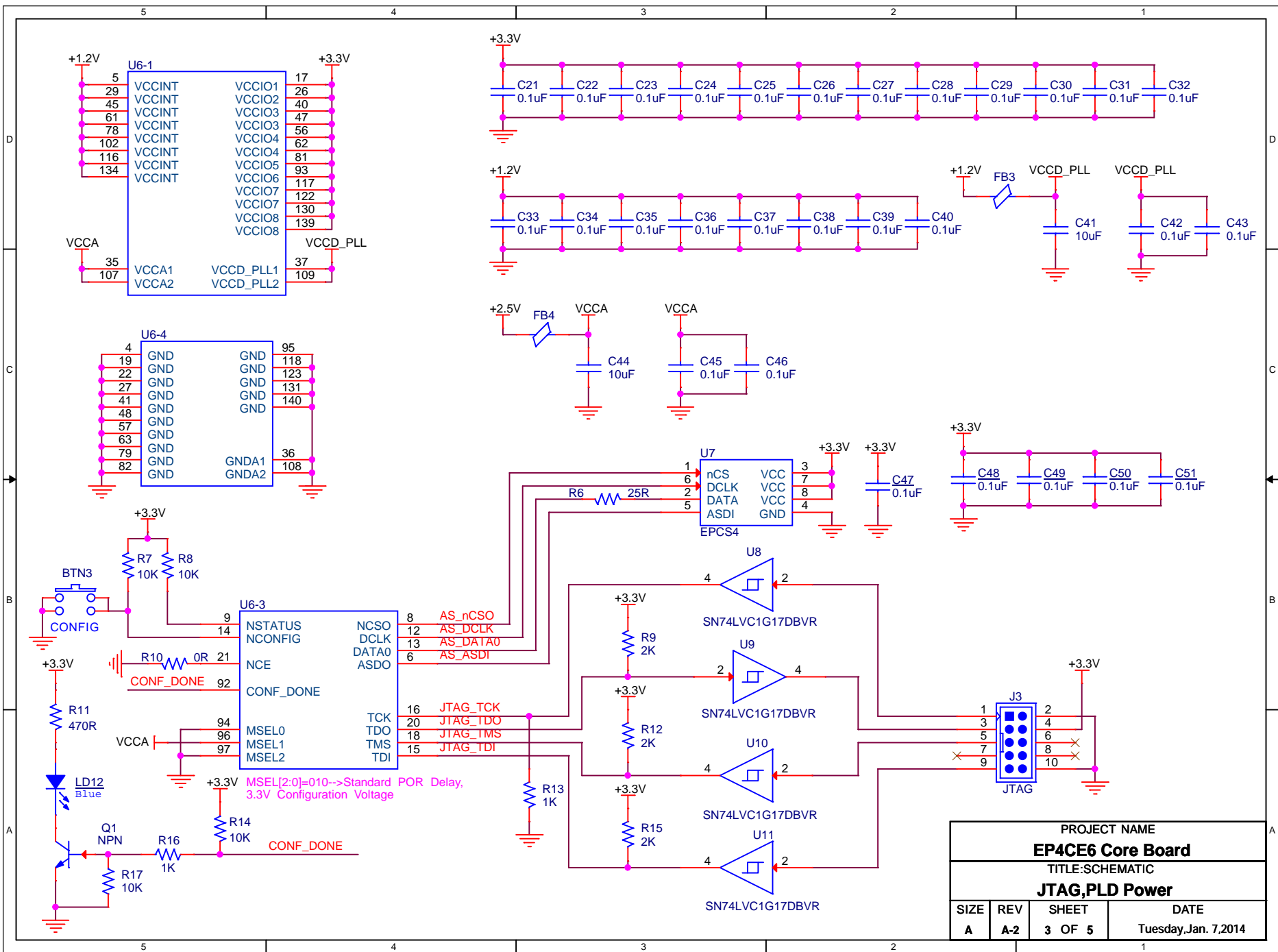


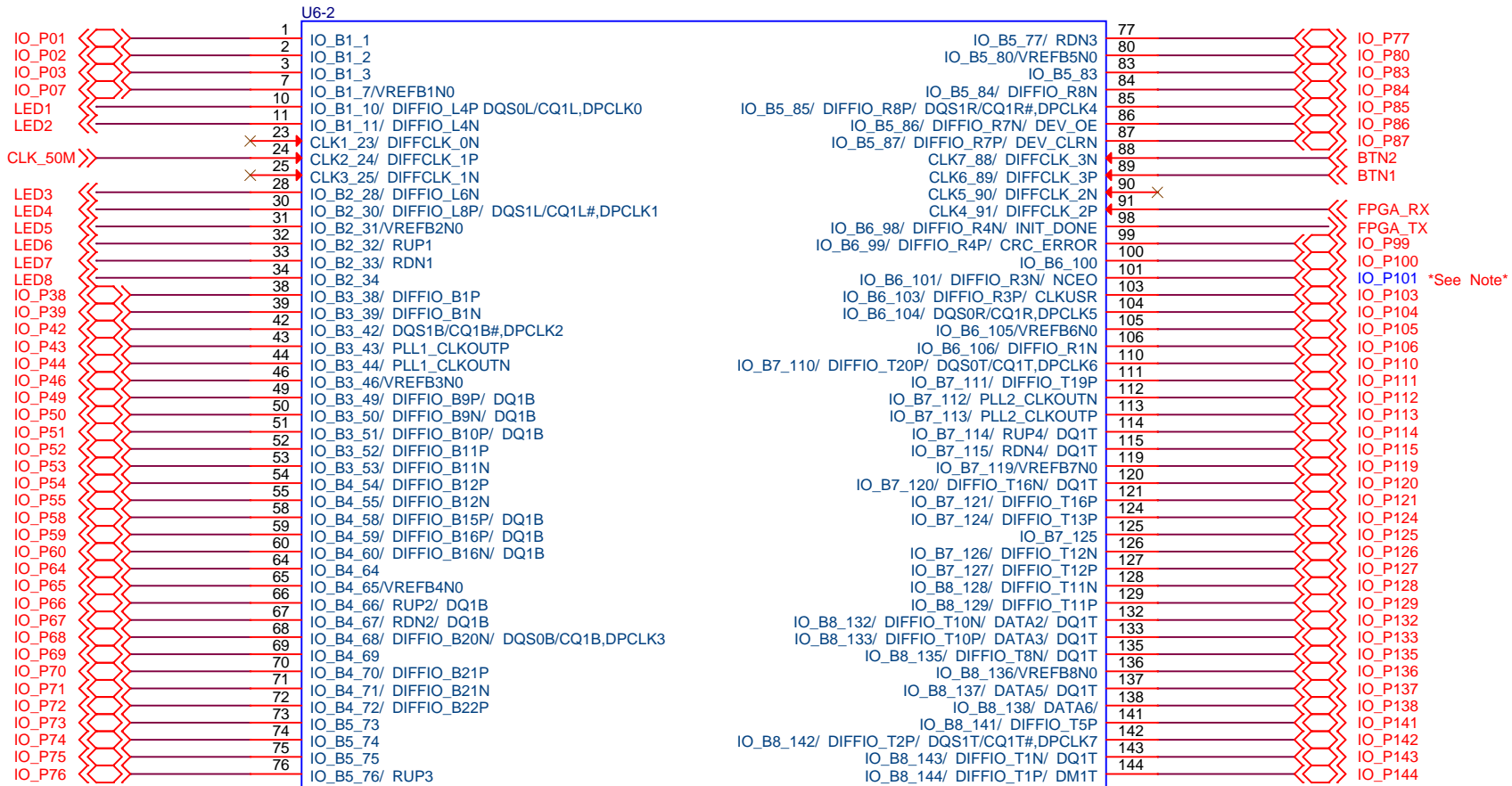
PROJECT NAME			
<b>EP4CE6 Core Board</b>			
TITLE:SCHEMATIC			
<b>Power,Clock</b>			
SIZE	REV	SHEET	DATE
A	A-2	1 OF 5	Tuesday,Jan. 7,2014



Default: LD10 Blink when data sent from PC to FPGA.  
 LD11 Blink when data sent from FPGA to PC.  
 User can configure the function of CBUS0,CBUS1 by programming the internal EEPROM using FT\_Prog from FTDI.



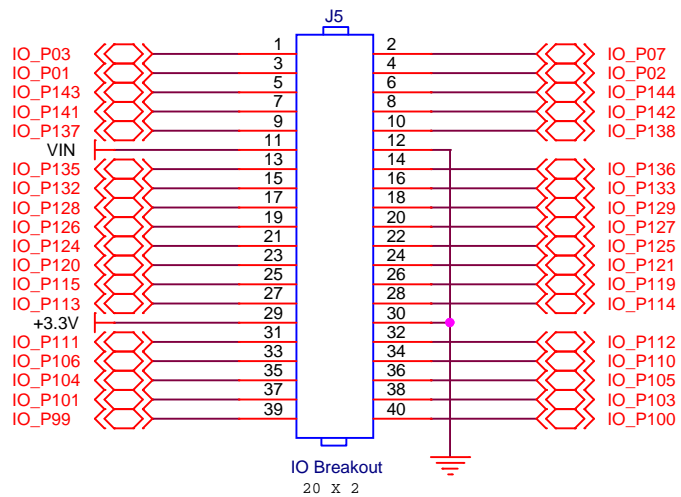
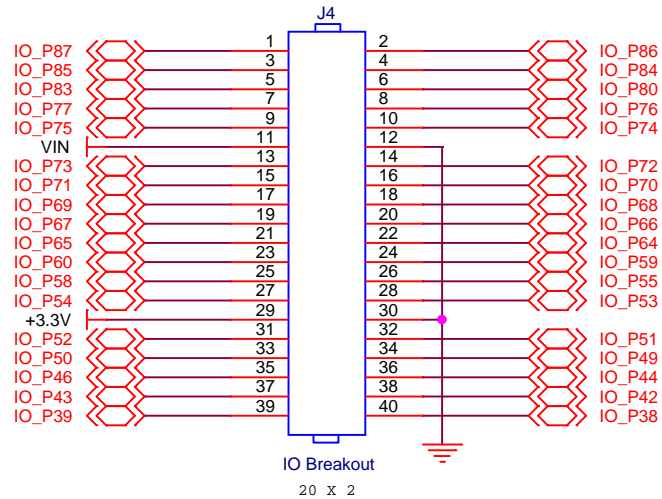
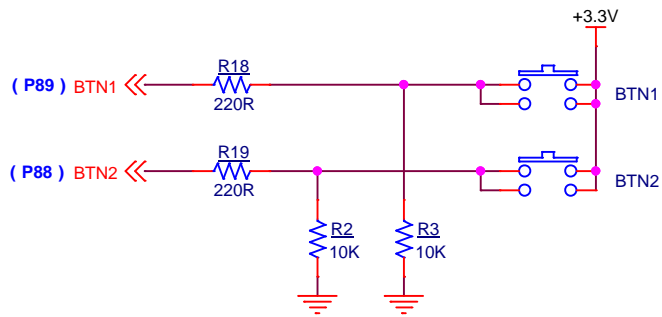
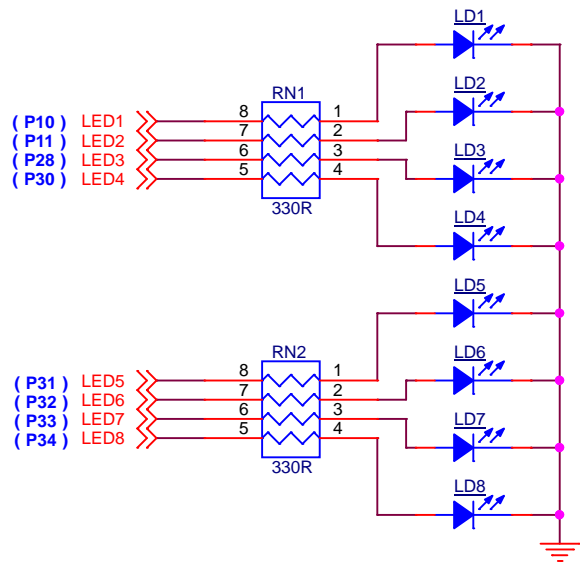
PROJECT NAME			
<b>EP4CE6 Core Board</b>			
TITLE:SCHEMATIC			
<b>JTAG,PLD Power</b>			
SIZE	REV	SHEET	DATE
A	A-2	3 OF 5	Tuesday, Jan. 7, 2014



**\*Note\***

PIN101 is set to nCEO function by default. To Configure it as an IO pin in a project, please follow the steps below :  
 Assignments --> Device --> Device and Pin Options --> Dual-Purpose Pins --> nCEO --> Use as regular IO

PROJECT NAME			
EP4CE6 Core Board			
TITLE:SCHEMATIC			
PLD IOs			
SIZE	REV	SHEET	DATE
A	A-2	4 OF 5	Tuesday,Jan. 7,2014



PROJECT NAME			
<b>EP4CE6 Core Board</b>			
TITLE:SCHEMATIC			
<b>LEDs,Buttons,IO Headers</b>			
SIZE	REV	SHEET	DATE
A	A-2	5 OF 5	Tuesday,Jan. 7,2014